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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,657	12/18/2001	Gilbert Wolrich	10559/613001/P12852	2667
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FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			PATEL, JAY P	
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			2616	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/024,657

Applicant(s)

WOLRICH ET AL.

Examiner

Jay P. Patel

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to the remarks filed 02/02/2006.
2. Claims 1-28 are pending.
3. Claims 1-28 are rejected.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6 and 21-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Calvignac et al. (US Patent 6658546 B2).
3. In regards to claim 1 and a method causing to receive in a queue manager a first enqueue or dequeue request with respect to a queue and causing to receive in the queue manager a second enqueue or dequeue request with respect to the queue, Calvignac teaches a data flow unit in figure 2 (see column 6, lines 18-22). The transmission controller within the data flow unit 201, comprises target blade queues (TBQs) 215. Calvignac discloses that frame control blocks (FCBs) that are queued in TBQs, can be dequeued from TBQs 215 by TBQ scheduler 228. Furthermore, TBQ scheduler may be configured to dequeue (first request) the next FCB from TBQs 215 and enqueue (second request) that FCB into PCB 230.

In further regards to claim 1 and causing to commence processing of the second request prior to completion of processing the first request, since the TBQ scheduler may be configured to dequeue the next FCB from TBQs 215 **and** enqueue that FCB into PCB 230, the enqueueing can occur in conjunction and before the commencement of dequeuing.

In regards to claim 2 and causing to modify stored information describing a structure of the queue in response to the requests because the data storage unit can store additional frame data, Calvignac teaches that once an entire data stored in the processed frame is read, the data storage unit 140 may store additional frame data (see column 6, lines 34-36).

In regards to claim 3 and causing the stored the modified information in a cache memory, Calvignac teaches that the data read by PCB 230, may be temporarily stored in data preparation are memory 214 (see column 6, lines 26-29). Furthermore, each slice of data 205, may represent a slice of memory (i.e DRAM) and the memory arbiter 204 may be configured to collect request (i.e, read, write) (see figure 2 and column 4, lines 54-56). Furthermore, each slice of memory can be configured to represent a slice in DRAM.

In regards to claim 4 and causing to store data related to the first and second requests using a linked list data structure, Calvignac teaches that different buffers comprising data of same frames may be linked together by means of pointers stored in BCBU 208 (Buffer control block unit) (see column 5, lines 14-16 and figure 2, BCBU 208).

In regards to claim 6 and the first request being a dequeue request and the second request being an enqueue request, TBQ scheduler may be configured to dequeue (first request) the next FCB from TBQs 215 and enqueue (second request) that FCB into PCB 230 (see column 6, lines 18-22).

4. In regards to claim 21 and commence processing of a received enqueue or dequeue request with respect to a queue prior to completion of processing a prior enqueue or dequeue request with respect to the same queue, Calvignac teaches that the TBQ scheduler may be configured to dequeue the next FCB from TBQs 215 and enqueue that FCB into PCB 230 therefore (see column 6, lines 18-22).

In regards to claim 22 and modifying stored information describing a structure of the queue in response to the requests because the data storage unit can store additional frame data, Calvignac teaches that once an entire data stored in the processed frame is read, the data storage unit 140 may store additional frame data (see column 6, lines 34-36).

In regards to claim 23 and storing the modified information in a cache memory, Calvignac teaches that the data read by PCB 230, may be temporarily stored in data preparation are memory 214 (see column 6, lines 26-29). Furthermore, each slice of data 205, may represent a slice of memory (i.e. DRAM) and the memory arbiter 204 may be configured to collect request (i.e., read, write) (see figure 2 and column 4, lines 54-56). Furthermore, each slice of memory can be configured to represent a slice in DRAM.

In regards to claim 24 and storing data related to the first and second requests using a linked list data structure, Calvignac teaches that different buffers comprising data of same frames may be linked together by means of pointers stored in BCBU 208 (Buffer control block unit) (see column 5, lines 14-16 and figure 2, BCBU 208).

In regards to claim 25 and commencing processing of the dequeue request prior to completion of processing the enqueue request, Calvignac teaches that TBQ scheduler may be configured to dequeue (first request) the next FCB from TBQs 215 and enqueue (second request) that FCB into PCB 230 (see column 6, lines 18-22).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 5, 7-8, 9-20 and 26-28 rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac as applied to claims 1 and 21 above, and further in view of Wilford et al. (US Patent 6687247 B1).

7. In regards to claims 5 and 26, Calvignac discloses all the limitations of claims 1 and 21 as stated above. Calvignac fails to exclusively disclose the first request being an enqueue request and the second request being a dequeue request. Wilford discloses the above-mentioned limitation.

Wilford discloses that in the inbound queue manger of figure 4 that the free block queue 415 holds queuing structures of pointer to packets stored in inbound packet buffer, which helps the enqueueing process (see column 9, lines 7-10). Wilford also reveals that queues are subsequently emptied by dequeue circuit 420 (see column 9, lines 34-37). Therefore, it would have been obvious to combine the teaching of a queue manager disclosed by Wilford with the enqueue and dequeue requests taught by Calvignac.

The proper motivation comes from Wilford where the motivation is to reduce packet latency and buffering delay (see last paragraph in the Background section in column 2).

In regards to claims 7 and 27, Calvignac discloses all the limitations of claims 1 and 21 as stated above. Clavignac fails to exclusively disclose the first and second requests both being enqueue requests. Wilford discloses the above-mentioned limitation.

Wilford discloses that the free block queue 415 is provides with 2064 queues arranged to prove eight distinct classes of service (see column 9, lines 11-16). Therefore, it would have been obvious to combine the teaching of the free block queue disclosed by Wilford with the enqueue and dequeue requests taught by Calvignac.

The proper motivation comes from Wilford where the motivation is to reduce packet latency and buffering delay (see last paragraph in the Background section in column 2).

In regards to claims 8 and 28, Calvignac discloses all the limitations of claims 1 and 21 as stated above. Clavignac fails to exclusively disclose the first and second request both being dequeue requests. Wilford discloses the above-mentioned limitation.

Wilford discloses that after queues are emptied, several queues are combined algorithmically by using deficit round robin or modified deficit round robin algorithms, into a single queue of packets (see column 9, lines 36-42). Since different classes of services exist and are emptied by dequeue circuit, there are more than one request for dequeuing packets. Therefore, it would have been obvious to combine the algorithm taught by Wilford with the enqueue and dequeue requests taught by Calvignac.

The proper motivation comes from Wilford where the motivation is to reduce packet latency and buffering delay (see last paragraph in the Background section in column 2).

8. In regards to claim 9 and a processing engine to make enqueue requests, Wilford discloses a linecard architecture for high speed routing of data in a communications device. The linecard architecture includes an inbound queue manager 240 that examines enqueued header portion of the packet to find out where to enqueue the packet (see figure 2, inbound receiver 220 and inbound queue manger 240, and column 5, lines 17-19 and lines 46-49).

In further regards to claim 9 and a scheduler to make dequeue requests, the linecard architecture also includes an outbound queue manager 280 (see figure 2 outbound queue manger 280). The outbound queue manger 280 further includes a

dequeue circuit 620, which dequeues the packets and sends them to the network interface (see figure 6, dequeue circuit 620 and column 11, lines 12-14).

In further regards to claim 9 and a cache memory to store data describing a structure of a queue, the linecard architecture further includes an inbound packet buffer 245 and an outbound packet buffer 285 to buffer the inbound and outbound packets respectively (see figure 2, packet buffers 245 and 285).

In further regards to claim 9 and anticipates a queue manger including a content addressable memory to store a reference to data in the cache memory describing the structure of the queue, the inbound and outbound queue managers, include a free block queue to hold queuing structure of pointers to packets stored in the inbound and outbound packet buffers respectively (see figure 4, free block queue 415, figure 6, free block queue 615 and column 9, lines 7-10).

In further regards to claim 9, Wilford fails to particularly, the queue manager configured to process the enqueue requests and the dequeue request and capable of commencing processing a request to a queue while a previous request with respect to the same queue is being processed. Calvignac discloses the above-mentioned limitation. Calvignac discloses that the PCB 230 may be configured to read a portion of the data stored in the processed frame in each particular read request. The entire data stored in the processed frame may be read in multiple read requests provided by PCB 230 (see column 6, lines 30-34 and figure 2 PCB 230). Therefore, it would have been obvious to combine the teaching of a multiple read requests disclosed by Calvignac with the queue manager apparatus taught by Wilford.

The proper motivation comes from Wilford where the motivation is to reduce packet latency and buffering delay (see last paragraph in the Background section in column 2).

In regards to claim 10, the inbound and outbound queue managers include packet buffers respectively; therefore, Wilford teaches a memory to store data placed in a queue (see packet buffers in figures 2, 4 and 6).

In regards to claim 11 and a plurality of multi-threaded pipelined programming engines, configured in a pipeline to receive, assemble and classify data packets to determine an output queue for each packet and to make request to the queue manager that specify the output queue, Wilford teaches that the output processing logic consists of a pipeline of several stages; When the DRAM read completes an entry is read from the Read Descriptor FIFO into the pipe, Cells are multiplexed into the pipe, Counts for the Request are fetched and any packet header sizes are inspected, Cells are counted, the lengths from any start of packet cells are added to totals and finally, totals are sent to the queue manager when a request completes and cell data is sent to the CPU (see column 43, lines 17-30).

In regards to claim 12, the teachings of Wilford used with regards to claim 11 are also relevant to claim 12.

In regards to claim 13 and the scheduler configured to determine the order of packets to be removed from the queue and to store a bit (empty state) for the queue indicating whether the queue is empty, Wilford discloses that the MDRR Scheduler

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maintains empty, back pressure, and in progress state for each output queue (see column 34, lines 14-16).

In regards to claim 14 and the queue manager configured to issue commands to return data describing the structure of the queue and to fetch data describing an updated structure of the queue from memory to ensure that data describing the structure of the queue stored in the cache memory is coherent with entries in the content addressable memory, the inbound and outbound queue managers, include a free block queue to hold queuing structure of pointers to packets stored in the inbound and outbound packet buffers respectively (see figure 4, free block queue 415, figure 6, free block queue 615 and column 9, lines 7-10).

9. In regards to claim 15 and a source of data packets and a destinations of data packets, Wilford teaches in figure 1 a communication network, an input interface 111, an inbound packet 111, an output interface 112 and an outbound packet 114 therefore, Wilford anticipates In further regards to claim 15, the control element 130 in figure 2 contains the circuitry to enqueue and dequeue inbound and outbound packets, respectively.

In further regards to claim 15 and a processing engine to make enqueue requests, Wilford teaches a linecard architecture for high speed routing of data in a communications device. The linecard architecture includes an inbound queue manager 240 that examines enqueued header portion of the packet to find out where to enqueue the packet (see figure 2, inbound receiver 220 and inbound queue manager 240, and column 5, lines 17-19 and lines 46-49).

In further regards to claim 15 and a scheduler to make dequeue requests, Wilford teaches that the linecard architecture also includes an outbound queue manager 280 (see figure 2 outbound queue manger 280). The outbound queue manger 280 further includes a dequeue circuit 620, which dequeues the packets and sends them to the network interface (see figure 6, dequeue circuit 620 and column 11, lines 12-14).

In further regards to claim 15 and a cache memory to store data describing a structure of a queue, Wilford teaches that the linecard architecture further includes an inbound packet buffer 245 and an outbound packet buffer 285 to buffer the inbound and outbound packets respectively (see figure 2, packet buffers 245 and 285).

In further regards to claim 15 and a queue manger including a content addressable memory to store a reference to data in the cache memory describing the structure of the queue, Wilford teaches that the inbound and outbound queue managers, include a free block queue to hold queuing structure of pointers to packets stored in the inbound and outbound packet buffers respectively (see figure 4, free block queue 415, figure 6, free block queue 615 and column 9, lines 7-10).

In further regards to claim 15, Wilford fails to particularly disclose the queue manager configured to process the enqueue requests and the dequeue request and capable of commencing processing a request to a queue while a previous request with respect to the same queue is being processed. Calvignac discloses the above-mentioned limitation. Calvignac discloses that the PCB 230 may be configured to read a portion of the data stored in the processed frame in each particular read request. The entire data stored in the processed frame may be read in multiple read requests

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provided by PCB 230 (see column 6, lines 30-34 and figure 2 PCB 230). Therefore, it would have been obvious to combine the teaching of a multiple read requests disclosed by Calvignac with the queue manager apparatus taught by Wilford.

The proper motivation comes from Wilford where the motivation is to reduce packet latency and buffering delay (see last paragraph in the Background section in column 2).

In regards to claim 16 and a memory to store data placed in a queue, Wilford teaches that the inbound and outbound queue managers include packet buffers respectively (see packet buffers in figures 2, 4 and 6).

In regards to claim 17 and a plurality of multi-threaded pipelined programming engines, configured in a pipeline to receive, assemble and classify data packets to determine an output queue for each packet and to make request to the queue manager that specify the output queue, Wilford teaches that the output processing logic consists of a pipeline of several stages; when the DRAM read completes an entry is read from the Read Descriptor FIFO into the pipe, Cells are multiplexed into the pipe, Counts for the Request are fetched and any packet header sizes are inspected, Cells are counted, the lengths from any start of packet cells are added to totals and finally, totals are sent to the queue manager when a request completes and cell data is sent to the CPU (see column 43, lines 17-30).

In regards to claim 18, the teachings used with regards to claim 17 are also relevant to claim 18.

In regards to claim 19 and the scheduler configured to determine the order of packets to be removed from the queue and to store a bit (empty state) for the queue indicating whether the queue is empty, Wilford teaches that the MDRR Scheduler maintains empty, back pressure, and in progress state for each output queue (see column 34, lines 14-16).

In regards to claim 20 and the queue manager configured to issue commands to return data describing the structure of the queue and to fetch data describing an updated structure of the queue from memory to ensure that data describing the structure of the queue stored in the cache memory is coherent with entries in the content addressable memory, Wilford teaches that the inbound and outbound queue managers, include a free block queue to hold queuing structure of pointers to packets stored in the inbound and outbound packet buffers respectively (see figure 4, free block queue 415, figure 6, free block queue 615 and column 9, lines 7-10).

Response to Arguments

10. Applicant's arguments filed 02/02/2006 have been fully considered but they are not persuasive.

11. In regards to claim 1, the applicant argues on page 3 that the enqueue and dequeue requests disclosed by Calvignac, are not received with respect to the same queue. The examiner however, disagrees. On column 6, lines 18-20, Calvignac states "FCBs queued in TBQs 215 may be scheduled to be dequeued from TBQs 215 by TBQ scheduler 228 and loaded into PCB 230." It is the examiner's interpretation that the

FCB that is queued in the TBQ 215 and then dequeued from the TBQ 215, that the enqueue and dequeue requests are with respect to the same queue.

In regards to the applicant alleging that Calvignac fails to suggest the second request occurring before the commencement of the first request, the examiner maintains that since the TBQ scheduler may be configured to dequeue the next FCB from TBQs 215 **and** enqueue that FCB into PCB 230, the enqueueing can occur in conjunction and before the commencement of dequeuing (see column 6, lines 18-22).

12. In regards to claim 2, the applicant argues that Calvignac fails to disclose storing additional information describing a structure of the queue. On column 6, lines 34-36 Calvignac states "Once the entire data stored in the processed frame is read, the data storage unit 140 may store additional framed data." Since the data is stored in frames, it is the examiner's interpretation that it is structured.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jay P. Patel whose telephone number is (571) 272-3086. The examiner can normally be reached on M-F 9:00 am - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jpp 4/13/06
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